REMARKS

Objections to Drawings

Proposed amended drawings are included herein. Changes are indicated by red ink. The drawings have been amended to include "Background Art" on FIGS. 15-19.

Claim Objections:

Claims 1 and 16 have been amended to address these objections.

Rejection of Claims 16-18 Under 35 U.S.C. §102(a) based on Applicants' Background Art (*Background Art*).

The invention of claim 16 is directed to a method of designing a protective circuit for a semiconductor device. Such a method includes executing a simulation with a predetermined charge device model (CDM) equivalent circuit, and selecting a ratio of the second resistance and the first resistance that prevents a potential between a gate and source/drain terminal of the first IGFET from exceeding a predetermined value.

Applicants' Background Art does not show the selection of a ratio between first and second resistances to prevent a gate to source/drain potential from exceeding a predetermined value. The Background Art describes the determination of a maximum value for an input resistance (argued to correspond to Applicants' first resistance) and a maximum value for a reference electric potential wiring (argued to correspond to Applicants' first resistance).[1] However, this does not meet the limitations of claim 16.

First, the determination of first and second maximum resistance values, as taught in the *Background Art*, is not described as being in relationship a maximum gate-to-source/drain potential. Second, these maximum resistance values are never described in relation with one another (e.g., a ratio). It is the inventors that have found that a CDM withstand voltage has a relationship with respect to the ratio of input resistance and a reference electric potential wiring (Rg/Rin).[2] Thus, any teachings regarding ratios of resistance values is arrived at with the benefit hindsight from Applicants' invention, and not from the *Background Art*.

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[1] See the Specification, Page 5, Line 21 to Page 6, Line 1.
[2] See the Specification, Page 14, Lines 7-14.

Accordingly, because claim 16 has limitations not shown in the *Background Art*, this ground of rejection is traversed.

Claim 17, which depends from claim 16, recites that a predetermined value of a potential between a gate source/drain terminal of a first IGFET is determined from a relationship between CDM test results and ratios of a second and first resistance. As noted above, the *Background Art* provides no teachings relating resistance ratios to performance, let alone teaching relating resistance ratios to the particular feature of CDM test results. Thus, this limitation is also lacking from the *Background Art*.

Rejection of Claims 1-20 Under 35 U.S.C. §103(a), based on *Background Art* in view of *Tailliet* (USP 5,515,226).

To establish a prima facie case of obviousness, a rejection must meet three basic criteria. First, there must be some suggestion or motivation to modify a reference or combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference(s) must teach or suggest all claim limitations.

A prima facie case of obviousness has not been established, as motivation for the proposed combination is lacking, and the cited combination of references does not show various limitations of the claims.

Motivation for the proposed combination is believed to be lacking. The *Background Art* relied upon in the rejection is directed to a charged device model (CDM) for an ESD event. The *Background Art* emphasizes the difference between CDM models and other models, such as the human body model (HBM) and machine model (MM).[3] *Tailliet* is directed to HBM and MM type events, and provides no teachings related to CDM events or models.[4] Thus, due to the differences in such models, the references teach away from such a combination, and thus the requisite motivation for the combination is lacking.

For this reason alone, the rejection of claims 1-20 is traversed.

In addition, or alternatively, a prima facie case of obviousness has not been established, as various claim limitations are not shown by the combination of references.

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[3] See the Specification, Page 5-10.

[4] See *Tailliet*, Col. 1, Lines 19-26.

The rejection of claims 1-15 will first be addressed.

The semiconductor integrated circuit device of claim 1 includes a plurality of IGFETs coupled to a corresponding I/O terminal through a corresponding first resistance. A first clamping circuit coupled to each I/O terminal. A second clamping circuit corresponding to each IGFET. Each second clamping circuit includes a second clamping device and the corresponding first resistance. Each second clamping device having a first terminal connected to a gate electrode of the corresponding IGFET and a second terminal connected to a source/drain terminal of the corresponding IGFET and a supply potential wiring. Each first clamping device is coupled to one second clamping device through a second resistance. At least two of the second clamping circuits vary from one another.

The combination of *APA* in view of *Tailliet* does not teach or suggest all limitations of claim 1. In particular, there is no teaching or suggesting at least two of the second clamping circuits that vary from one another, as recited in claim 1.

It is admitted in the rejection that the *Background Art* does not disclose that at least two of the second clamping circuits vary from one another.[5]

However, the other reference relied upon by the rejection, *Tailliet* does not show such a limitation, either. *Tailliet* discloses an electrostatic discharge protection circuit with a first voltage limiter (argued to correspond to Applicants' first clamping device) and a second voltage limiter (argued to correspond to Applicants' first clamping device).[6] However, *Tailliet* only discloses that a second voltage limiter has a size ratio that is different than the first voltage limiter.[7] *Tailliet* is silent about variations or lack of variations between second voltage limiters corresponding to different pads.

For this reason, *Tailliet* is not believed to show or be suggestive of second clamping circuits that vary from one another, as recited in claim 1. Thus, because the cited combination of references does not show all limitations of claim 1, a prima facie case has not been established, and the rejection of claims 1-15 is traversed.

Various claims depending from claim 1 are believed to include additional limitations not shown by the cited combination.

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[5] See the Office Action dated 10/7/2002, page 4.

[6] See *Tailliet*, FIG. 3, which shows first voltage limiter (EC1j) and a second voltage limiter (EC2j).

Claim 3 recites that at least two second clamping devices vary by having second clamping circuits with different capabilities. Claim 15 recites second clamping devices with different construction.

As noted above, *Tailliet* provides no description of how one voltage limiter may or may not differ from another, let alone show such limiters differ in capability. Thus, the combination of references is not believed to be suggestive of the limitations of claim 3 or 15, either.

Claim 4 recites that a first resistance of one second clamping circuit is different than a first resistance of another second clamping circuit. The *Background Art* shows examples of multiple I/O arrangements that include multiple input resistances Rin (argued to correspond to Applicants' first resistance values).[8] However, such input resistance values are never described as being different from one another. In rejecting claim 4, the rejection cites a portion of the *Background Art*. However, the cited portion refers to a reference electric potential wiring Rg and not an input resistance Rin. It is noted that such an electric potential wiring Rg (Rg) does not couple an IGFET to an I/O terminal, as is the case for Applicants' first resistance (see claim 1).

Claim 8 recites that a majority of at least one first resistance includes non-wiring structures. Claim 9 indicates that a first resistance includes an effective channel resistance of an input path IGFET. The rejection of claims 8 and 9 relies on the following rationale.

> [The *Background Art*] discloses that the first resistance R114 includes an effective channel resistance of an input path transistor (end to end path through the transistor 112a).[9]

Applicants' *Background Art* indicates that an input resistor (e.g., 114) is illustrative of an input resistance and an input wiring resistance inherent in a semiconductor device. Nothing in Applicants' *Background Art* indicates that a transistor that is being protected (i.e., 112) is included in an input resistance. Clarification for the basis of this rejection is respectfully requested.

Claim 12 adds the limitation that a second terminal of each second clamping device is

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[7] See *Tailliet*, Col. 5, Lines 10-16.
[8] See the Specification, FIGS. 17 and 18, which show input resistances 114a to 114c.
[9] See the Office Action, dated 10/7/02, Page 6, Lines 5-7.

connected to a second supply terminal different from a first supply terminal. Applicants' *Background Art* shows an example in which electrostatic protective devices are connected to one wiring, while CDM protective devices are connected to another wiring. However, such wirings are connected to the same supply terminal, and not different supply terminals, as recited in claim 12.[10]

Thus, because the combination does not show or suggest all limitations of claim 12, a prima facie case of obviousness has not been established for this claim.

The rejection of claims 19 and 20 will now be addressed.

To the extent that this ground of rejection relies on the *Background Art*, the comments set forth above for claim 16 are incorporated by reference herein. Namely, that the *Background Art* does not show or suggest selecting a ratio of the second resistance and the first resistance that prevents a potential between a gate and source/drain terminal from exceeding a predetermined value.

Claims 1 and 16 have been amended to address informalities and not in response to the prior art. The present claims 1-20 are believed to be in allowable form. It is respectfully requested that the application be forwarded for allowance and issue.

Respectfully Submitted,

Darryl G. Walker January 3, 2003

Darryl G. Walker
Attorney
Reg. No. 43,232

Darryl G. Walker
Attorney/Agent
300 South First Street
Suite 235
San Jose, CA 95113
Tel. 1-408-289-5314

[10] See the Specification, FIG. 18 which shows two wirings 118 and 119 connected to the same supply terminal 115. This is in contrast to Applicants' embodiment of FIG. 3, which shows one very particular example of two different supply terminals 15a and 15b.

Version With Markings to Show Changes Made

In the Claims.

1. (Amended) A semiconductor integrated circuit device, comprising:

a plurality of insulated gate field effect transistors **[(IGFETs)]** **IGFETs** coupled to a corresponding input/output (I/O) terminal through a corresponding first resistance;

a first clamping device coupled to each I/O terminal;

a second clamping circuit corresponding to each IGFET, each second clamping circuit including a second clamping device and the corresponding first resistance, each second clamping device having a first terminal connected to a gate electrode of the corresponding IGFET and a second terminal connected to a source/drain terminal of the corresponding IGFET and a supply potential wiring;

each first clamping device being coupled to one second clamping device through a second resistance; and

at least two of the second clamping circuits vary from one another.

16. (Amended) A method for designing a protective circuit for a semiconductor integrated circuit device that includes insulated gate field effect transistors **[(IGFETs)]** **IGFETs** formed thereon, the method comprising the steps of:

executing a simulation with a predetermined charged device model (CDM) equivalent circuit that includes a first clamping device connected to an input/output (I/O) terminal, a first IGFET having a gate connected to the I/O terminal through a first resistance (Rin), a second clamping device connected between gate and source/drain terminals of the first IGFET and connected to a supply potential wiring, the first and second clamping devices being connected to one another through a second resistance (Rg); and

selecting a ratio of the second resistance and the first resistance (Rg/Rin) that prevents a potential between the gate and source/drain terminal of the first IGFET from exceeding a predetermined value.